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Simulation and Finite Element Analysis of Electrical Characteristics of Gate-all-Around Junctionless Nanowire Transistors

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Gate all around nanowire transistors is one of the widely researched semiconductor devices, which has shown possibility of further miniaturization of semiconductor devices. This structure promises better current controllability and also lowers power consumption. In this paper, Silicon and Indium Antimonide based nanowire transistors have been designed and simulated using Multiphysics simulation software to investigate on its electrical properties. Simulations have been carried out to study band bending, drain current and current density inside the device for changing gate voltages. Further analytical model of the device is developed to explain the physical mechanism behind the operation of the device to support the simulation result.

Keywords: Nanowire, Multiphysics, Current controllability

PACS numbers: 62.23.Hj, 85.30.Tv, 07.05.Tp, 85.30. – z

1. INTRODUCTION

All the electronic devices are now being scaled down from the micrometer range to nanometer range owing to the overwhelming demand for reduced power consumption and increased speed of the gadgets that we use in our daily life. This calls for devices that have superb gate performance where the current in the channel can be controlled with lower gate voltages. This gave rise to the need of studying the electron physics of these devices at reduced gate lengths. One such device is the Gate All Around (GAA) Nanowire Transistor (NWT) [1-5]. It has the dielectric gate wrapped all around its channel for marvelous current control in the channel.

A lot of emphasis has already been laid on analyzing Silicon GAA NWT [1-6] and were found to be good replacement for conventional MOSFET in CMOS designs. Later, III-V compound semiconductors such as GaAs, InAs, InSb, GaN [7-10] were also considered for these applications. GAA architecture allows superior control over the channel current. In junctionless nanowire transistor (JNT) there is no junction between source, channel, and drain. Thus, it is easy to fabricate it. Also, it's immunity to short channel effect is very high. Also doping concentration is same throughout the source, drain and channel. But, due to very high doping, its drive current gets limited and thus, it is having low mobility. To improve the mobility, compound semiconductor based GAA JNT is used. Also compound semiconductor based nanowires can be used for high frequency applications.

This paper studies the GAA NWT with Si and InSb being its constituent element independently. Comparison of the energy band diagrams of both have been carried out. With change in gate voltage the shift in conduction band and valance band energy levels is clearly shown. Current voltage characteristics have been shown of both the devices. The current density of both the devices is also been portrayed in this paper. Superior current transport capability as shown here implies the use of nanowire transistors in sub 20 nm gate length and considered for futuristic device applications. InSb nanowire transistor has shown better performance as compared to Si based nanowire transistor.

2. DEVICE STRUCTURE AND PARAMETERS

The GAA NWT has been considered with Si and InSb being its constituent materials one by one. The doping levels for both the NWT has been kept the same for uniform consideration and study. The source and drain region has been doped with a donor concentration of $10^{26}/m^3$ and the channel has been doped with an acceptor impurity of $10^{23}/m^3$. The length of the source and drain has been kept constant for both the devices at 10 nm and the gate length or the channel length has been kept at 20 nm. While consideration of the insulator layer over the gate, SiO_2 has been taken as the material with a gate thickness of 2 nm and the dielectric constant being 3.9. A low thickness of the gate imparts better channel controllability of the device. Figure 1 shows the structure of JNT.

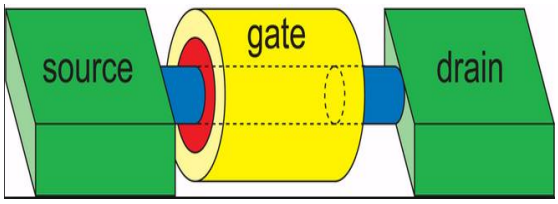

Fig. 1 – Structure of cylindrical GAA nanowire transistor

2.1 Analytical model

Two dimensional Poisson's equations with cylindrical coordinates are used for developing the analytical model [11] given as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\varphi_i(r,z)\right)+\frac{\partial^2}{\partial z^2}\varphi_i(r,z)=-\frac{qN_D}{\epsilon_j} \qquad (1)$$

where r is the radial distance, z is the position along the channel, $\varphi_i(r,z)$ is the potential of the material

depending on radius and position along the channel, N_D is the doping concentration.

Here, we use the superposition approach in which the potential function is decomposed into two parts i.e., 1-D solution $W(r)$ and 2-D solution $V(r, z)$ and is written as,

$$\varphi(r,z) = W(r) + V(r,z) \tag{2}$$

$W(r)$ and $V(r, z)$ can be written as:

$$\frac{\partial^2}{\partial r^2}W(r) + \frac{1}{r}\frac{\partial}{\partial r}W(r) = -\frac{qN_D}{\epsilon_j} \tag{3}$$

$$\frac{\partial^2}{\partial r^2}V(r,z) + \frac{1}{r}\frac{\partial}{\partial r}V(r,z) + \frac{\partial^2}{\partial z^2}V(r,z) = 0 \tag{4}$$

Parabolic approximations is considered for solving 1-D equation (3) and is given as:

$$W(r) = a + br + cr^2 \tag{5}$$

Boundary conditions used for solving (5) are:

- Electric field at the centre of the channel is zero in junctionless transistor:

$$\frac{\partial}{\partial r}\Phi(r,z)|_{r=0} = 0 \tag{6}$$

- Electric field at the interface between channel and the gate interface is:

$$\frac{\partial}{\partial r}\Phi(r,z)|_{r=R} = \frac{C_{ox}}{\epsilon_j}[V_{gs} - V_{fb} - \Phi(r=R,z)] \tag{7}$$

Where V_{gs} is the gate to source voltage, V_{fb} is the flatband voltage and C_{ox} is the oxide capacitance.

Using the above boundary conditions, solution of 1-D Poisson's equation is obtained as:

$$W_i(r) = V_{gs} - V_{fbi} - \frac{qN_D}{4\varepsilon_j}r^2 + \frac{qN_D R}{2C_{ox}} + \frac{qN_D R^2}{4\varepsilon_j} \tag{8}$$

Now considering 2-D equation (equation (4)), solution of 2-D Poisson's equation is similar to Laplace equation. And, the general solution of Laplace equation in cylindrical co-ordinates is given as:

$$V(r,z) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} J_m(\alpha_{mn}r)\left(A_{mn}e^{k_{mn}z} + B_{mn}e^{-\alpha_{mn}z}\right)\times \\ \times(C_{mn}\,\mathrm{Cos}\,m\phi + D_{mn}\,\mathrm{Sin}\,n\phi) \tag{9}$$

Where, J_m is the Bessel's function of order m, α_n is the Eigen vector satisfying equation $\alpha_n J_1(\alpha_n r) = \beta J_0(\alpha_n r)$. A and B are the coefficients whose values can be predicted using some boundary conditions. Keeping only terms with $m = 0$ because in cylindrical geometry, potential cannot depend on ϕ. Thus, the equation obtained is:

$$V(r,z) = \sum_{n=0}^{\infty} J_0(\alpha_n r)\left(Ae^{\alpha_n z} + Be^{-\alpha_n z}\right) \tag{10}$$

For solving the potential equation (10) and solving the value of coefficients A and B, boundary conditions used at source and drain end are:

(i) The potential at the source end is

$$\varphi(r,z)|_{z=0} = V_R$$

(ii) The potential at the drain end is

$$\varphi(r,z)|_{z=L} = V_R + V_{ds}$$

Where, V_R is the reference potential

Values of A and B can easily be obtained using the above boundary conditions.

Finally current can be obtained from:

$$I_{ds}(z) = \pi t_{si}\int_0^{\frac{t_{si}}{2}} J_i(r,z)dr \tag{11}$$

As we know, current density consists of drift current density and diffusion current density. Thus, it can be expressed as:

$$J_i(r,z) = -q\mu n(r,z)\frac{\partial\varphi_i(r,z)}{\partial z} \tag{12}$$

Substituting eq. (12) in eq. (11) drain current can easily be computed.

2.2 Simulation Model

While performing Multiphysics simulation the following generalized equations are considered by the software for computation of potential and current.

$$\nabla.(-\epsilon_r\nabla V) = q(p - n + N_d^+ - N_a^-$$
$$\nabla.J_n = -qU_n$$
$$\nabla.J_p = qU_p$$
$$J_n = qn\mu_n\nabla E_c + \mu_n k_b TG\left(\frac{n}{N_c}\right)\nabla n + qnD_{n,th}\nabla ln(T)$$
$$J_p = qp\mu_p\nabla E_v + \mu_p k_b TG\left(\frac{p}{N_v}\right)\nabla p + qpD_{p,th}\nabla ln(T)$$
$$E_c = -(V + \chi_0)$$
$$E_v = -(V + \chi_0 + E_{g,0})$$

The various terms used above are self explanatory and can be modified by the user as per analyses performed.

3. RESULTS AND DISCUSSION

While carrying out the simulations, the structure of the nanowire has been considered to be a 2-D asymmetric one and Fig. 2 shows one half of the device. The parameters considered for the device are given in Table 1.

Table 1 – Values of various parameters used in simulation

Parameters	Value
Nanowire Radius	10 nm
Length of Channel	20 nm
Length of Source/Drain	10 nm
Thickness of Oxide Layer	2 nm
Acceptor Concentration	1E23[1/m^3]
Donor Concentration	1E26[1/m^3]

Both Silicon and Indium Antimonide (InSb) based junctionless nanowire transistor is considered in the analysis.

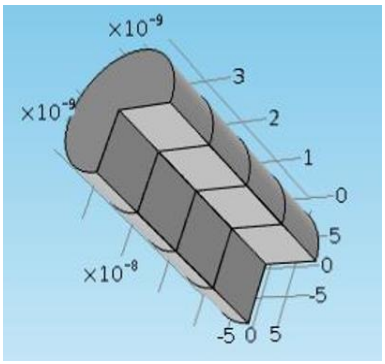

Fig. 2 – The cylindrical structure of junctionless nanowire transistor as designed in Multiphysics Simulation Software

Fig. 3 shows the doping profile for Silicon NWT. It can be observed that the concentration of electrons is highest at the source and drain. The concentration keeps on decreasing after the boundaries of the source and drain towards the channel as the channel region is doped with an acceptor concentration. The doping level of the channel is very low and can be considered to be an undoped one. The doping profile is an important aspect of any device as it brings about the desired current levels. It also defines the electric field vectors in the device.

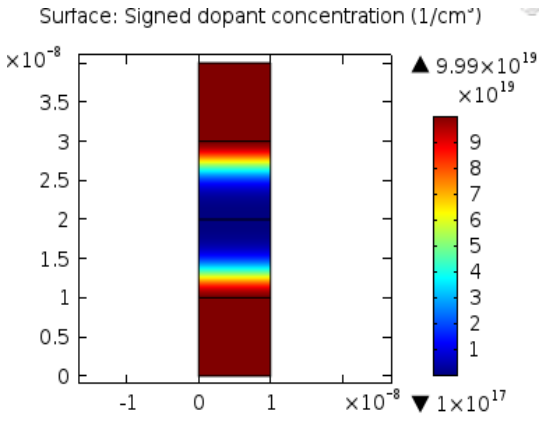

Fig. 3 – Doping concentration of Si Nanowire Transistor

Fig. 4(a) and (b) illustrates the energy band diagram of both the devices considered one by one. The band diagrams are along the radius of the circular cross-section where the centre is 0nm and the radius increases as 10 nm along all sides. Both the band diagrams show the position of conduction band and the valence band. Both the band diagrams are considered when the device is on the on state and the gate voltage is varied from 0 V to1.5 V. When voltage at the gate i.e., V_G is applied, the conduction band shifts which leads to increased electron density and hence an increased value of current in the channel under the gate region. It can be observed from the diagrams that the band gap of Silicon is 1.12 and that of InSb is 0.17 V. The band gap of InSb being smaller, conduction is much more easier in InSb than Si at nominally lower temperatures. Lower gate voltages will be able to switch on the device in the case of InSb. Thus it would be more power efficient than Si in cases where lower band gap won't hinder the operation as in the case of high temperature operations. Also electron and hole quasi fermi level shifts as per the applied voltage.

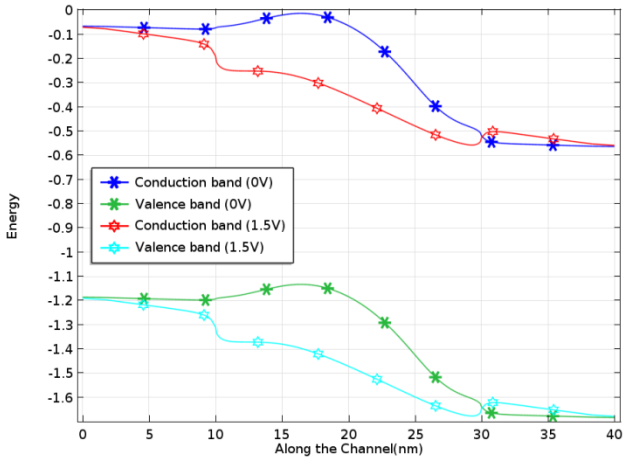

Fig. 4a – Band diagram with the variation in applied gate voltage (Si)

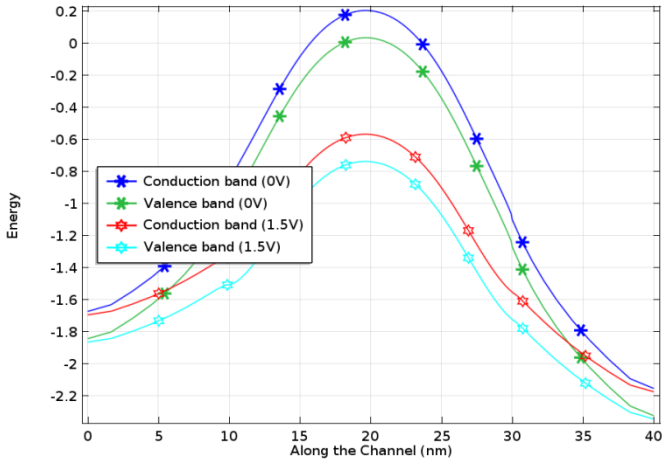

Fig. 4b – Band diagram with the variation in applied gate voltage (InSb)

Fig. 5(a) and 5(b) elaborate on the transfer characteristics of the device. The substantial difference is between the two devices is the markings on the current, where the values of current in InSb is nearly twice the hundred times the current in silicon NWT at the same gate voltage. This agrees very well with our conclusions on the energy band diagram. Both the simulations have been carried out at a variable drain voltage. Transconductance being the ratio of change in I_D to ratio of change in V_G in the same interval is higher in the case of InSb than Si and hence can be an excellent candidate for amplifying procedures.

Fig. 6(a) and 6(b) describe the current density in A/m² for both the Si and InSb nanowires. It can be again observed that there is a difference in order of the current density by 2. The reason for considering the current density along the mid axis of the nanowire is because of the structure of the nanowire. Since the gate is all around the channel, unlike the single gate conventional MOSFET conduction is across along the complete channel. Hence, if current density has to be considered then the current along all the points from the centre of the cylindrical channel towards the surface has to be considered on all sides. The nanowire has a radius of 10 nm and since the channel is cylindrical, its

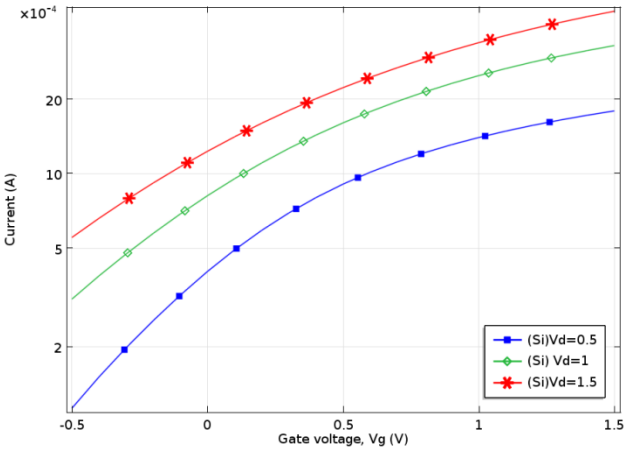

Fig. 5a – Variation of current with gate voltage for different values of drain voltages (Si)

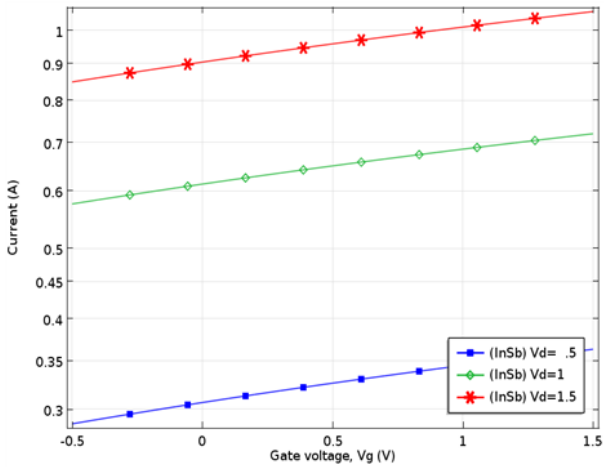

Fig. 5b – Variation of current with gate voltage for different values of drain voltages (InSb)

cross-section is a circle with a radius of 10 nm. The plots show the current density along the radii of both the nanowires. Since the gate is at the outermost surface of the cylindrical channel, current density is expected to be highest at the surface just below the gate and that can be observed from the figures also. Thus, the current is least at the central axis of the cylindrical channel and keeps on increasing along all the sides towards the surface in the direction outwards from the central axis.

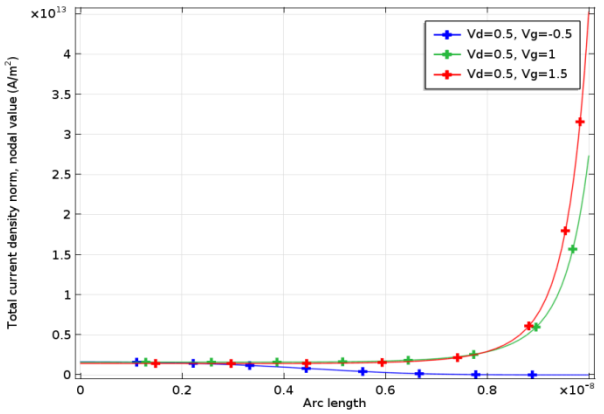

Fig. 6a – Current density along the arc length in Si nanowire

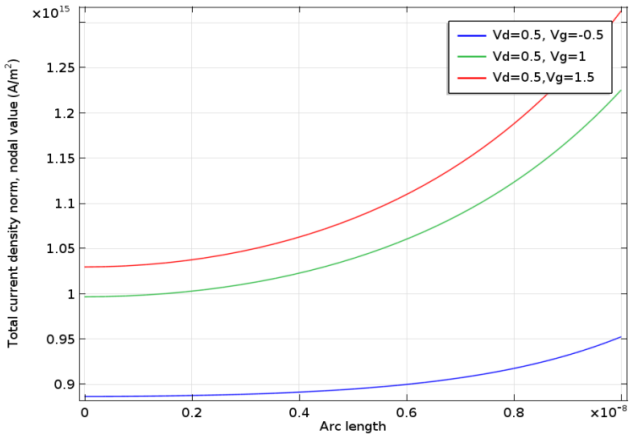

Fig. 6b – Current density along the arc length in InSb nanowire

Next, the trap occupancy in the channel under the gate region is being discussed. For simulation purpose, we have chosen trap density to be $5 \times 10^{16}/m^3$. Trap occupancy will be observed in terms of probability, where the highest value one (1) denotes that all traps are occupied as shown in Fig. 7. The total length of the material is about 40 nm including the source, drain and channel. The channel varies between 10 nm and 30 nm on the z-axis and hence only that region is considered in the trap occupancy as the gate is above the channel only and the traps are introduced by the coupling between the two.

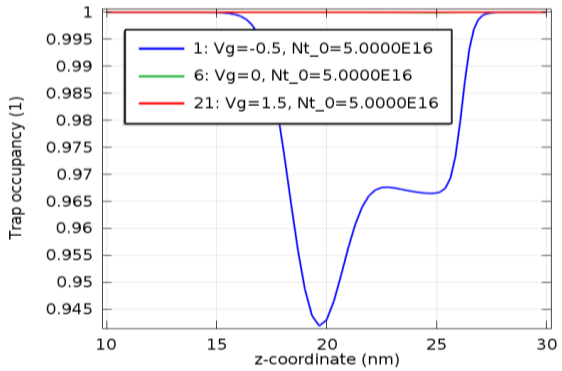

Fig. 7 – Trap density in NWT with SiO_2 as the gate material

The trap occupancy can be appreciated when considering the switching applications and when using these devices for CMOS where high speed switching is necessary. When the voltage is 0 V or 1.5 V it can be observed that almost all the traps are occupied. The reason can be attributed to the fact that at 0 V the device is at dynamic equilibrium and hence all traps are occupied. At 1.5 V, all the electrons in the channel travel along the channel and near the surface of the nanowire. This is the reason why all the traps are occupied at 1.5 V, since traps are located under the gate and near the surface. Now, when a negative voltage is applied, the trap densities become more evident. The reason for this phenomenon can be attributed to the fact that when a negative gate voltage is applied to the gate, electrons are 'pushed' away from the surface towards the centre of the nanowire from all the sides as the shape is cylindrical. Due to this phenomenon, trap occupancy goes down when negative voltage is applied.

Now, the important fact to be noted here is that trap occupancy should be low when negative voltage is applied or else it defies the notion of switching where reverse voltage should drive the device to off state. With SiO_2 as the gate material, the lowest trap density is 0.940 in the middle of the channel, which means that 94 % of the traps are still occupied in the channel when the device is supposed to be in the off state

4. CONCLUSIONS AND FUTURE SCOPE

An analysis of InSb and Si GAA junctionless NWT has been carried out which shows clearly that the channel current (drain current) is much higher in InSb than Si at same gate voltages. This makes it viable for very low voltage amplification purposes like sensors where the signal procured by the sensors may be very low to be of any use for any further analysis. But using InSb nanowires can enable proper amplification of the signals to make it useful for further processing. This device can be used at operations which operate at room temperatures where conduction can occur easily. Using it at higher temperatures may pose a problem such as band gap narrowing to such extents that controlling the current can become difficult. Such problems can occur with other compound elements such as Indium Arsenide (InAs). But these problems can be resolved by using high-k dielectrics or by using gate stacks. Also, high-k dielectrics are a good gate material for switching applications in the digital application where the switching efficiency is most important.

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